Documentation Standards

Thank John Wakerly for providing his slides and figures.
Documentation Standards

- Specification
- **Block diagrams**
  - First step in hierarchical design
- **Schematic diagrams**
- HDL programs (ABEL, Verilog, VHDL)
- **Timing diagrams**
- Circuit descriptions
Block diagram

- Functional modules
- Inputs
- Outputs
- Internal datapath
- Control signals

Flow of data and control should be clearly indicated

Bus: a collection of two or more related signals
Double or heavy lines
Or INBUS[31..0]
Schematic diagrams

- Details of component inputs, outputs, and interconnections
- Reference designators
  - Specifies a particular instance of an IC, e.g., U12
- Pin numbers
- Names for all signals
- Page-to-page connectors

Logic diagram does not give all the details
Example schematic
Flat schematic structure
Hierarchical schematic structure
Line crossing and connections

Crossing

Connection

Connection
Gate symbols

- **AND**
- **OR**
- **BUFFER**
- **NAND**
- **NOR**
- **INVERTER**

Diagram of gate symbols
DeMorgan equivalent symbols

Which symbol to use?

Answer depends on signal names and active levels.
Active levels

• Signal names are chosen to be descriptive

• Active levels – HIGH or LOW
  – Named condition or action occurs in the HIGH state, we use active-high signal names
  – Named condition or action occurs in the LOW state, we use active-low signal names

If a signal is named as PASS, what does it mean if it is HIGH?
Signal names

- To avoid confusion, signal name indicate active level

<table>
<thead>
<tr>
<th>Active Low</th>
<th>Active High</th>
</tr>
</thead>
<tbody>
<tr>
<td>READY–</td>
<td>READY+</td>
</tr>
<tr>
<td>ERROR.L</td>
<td>ERROR.H</td>
</tr>
<tr>
<td>ADDR15(L)</td>
<td>ADDR15(H)</td>
</tr>
<tr>
<td>RESET*</td>
<td>RESET</td>
</tr>
<tr>
<td>ENABLE~</td>
<td>ENABLE</td>
</tr>
<tr>
<td>~GO</td>
<td>GO</td>
</tr>
<tr>
<td>/RECEIVE</td>
<td>RECEIVE</td>
</tr>
<tr>
<td><strong>TRANSMIT_L</strong></td>
<td><strong>TRANSMIT</strong></td>
</tr>
</tbody>
</table>
Signal name example

- **HIGH** when error occurs
  - Error Circuit
  - ERROR
  - OK_L
- **LOW** when error occurs
  - Error Circuit
  - ERROR_L
  - ERROR
  - ERROR1_L
Example

\[ \text{GO} = \text{READY} \cdot \text{REQUEST} \]

Bubble-to-bubble design: choose logic symbols, signal names, and active-level that make the function of a logic circuit easier to understand
Active levels for pins

AND, OR, and a complex logic element

Same elements with active-low inputs and outputs
Be careful !!
Other documentation

- Timing diagrams
  - Output from simulator
  - Specialized timing-diagram drawing tools

- Circuit descriptions
  - Text (word processing)
  - Can be as big as a book (e.g., typical Cisco ASIC descriptions)
  - Typically incorporate other elements (block diagrams, timing diagrams, etc.)
Timing diagram for a combinational circuit

```
  GO       READY
  |       |
ENB     DAT
  |       |
```

GO

READY

DAT

\[ t_{\text{RDY}} \]

\[ t_{\text{DAT}} \]
Low-going and high-going transitions

- Low-going transitions
- High-going transitions
Certain and uncertain transitions

WRITE_L

DATAIN

must be stable

DATAOUT

old

new data

\( t_{\text{setup}} \)

\( t_{\text{OUTmin}} \)

\( t_{\text{OUTmax}} \)

\( t_{\text{hold}} \)

High or low-going transitions
Sequence of values on an 8-bit bus

CLEAR

COUNT

STEP[7:0]  00  01  02  03
Circuit descriptions

• A narrative text document explains how the circuit works internally
  – Define terms and acronyms
  – All the assumptions
  – Nonobvious tricks
  – Potential pitfalls in the design and operations