MPC875 Cache

In this lab we explore the MPC875 caches and conduct an empirical study of cache performance. MPC875 has separate instruction and data caches. The data cache is a two-way associative cache that uses physical addresses. The cache has 16-byte line size. MPC875 allows programs to control caches explicitly, using the `mtspr` and `mfspr` instructions to read from or write to special purpose registers (SPRs). There are two sets of three registers: one for data cache and one for instruction cache. These registers are listed below. Read the manual for detailed descriptions.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>SPR number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC_CST</td>
<td>568</td>
<td>Data cache control and status register</td>
</tr>
<tr>
<td>DC_ADR</td>
<td>569</td>
<td>Data cache address register</td>
</tr>
<tr>
<td>DC_DAT</td>
<td>570</td>
<td>Data cache data register</td>
</tr>
<tr>
<td>IC_CST</td>
<td>560</td>
<td>Instruction cache control and status register</td>
</tr>
<tr>
<td>IC_ADR</td>
<td>561</td>
<td>Instruction cache address register</td>
</tr>
<tr>
<td>IC_DAT</td>
<td>562</td>
<td>Instruction cache data register</td>
</tr>
</tbody>
</table>

1 Cache performance

You will experiment with the cache and related control registers in this exercise and evaluate its impact on performance.

1.1 Reading the time base register

MPC875 has a 64-bit time base register (TBU and TBL). The lower 32 bits (TBL) are enough for the timing purpose in this lab. The time base register increases at the same clock rate as the decrementer register. The default rate is 2.5 MHz on the board we are using. You need to enable the time-base registers (reusing the code you developed in previous labs).

1.2 Timing a loop

Write an empty loop with `bdnz` instruction and test how much time an iteration takes. Basically, you can read the time base register twice, once before and once after the loop, and their difference is the time that the loop takes. Note that the MPC875 runs at 120 MHz (the default setting). So you should run the loop long enough to measure the execution time with 2.5 MHz time base registers. It is also recommended to write the loop with embedded instructions so you know what instructions are executed.

1.3 Timing an ALU instruction

Add a single ALU instruction in the empty loop and test how much time an iteration takes now. Given the clock rate of 120 MHz, how many cycles does an ALU instruction take?

1.4 Timing an load instruction

Add a single memory load instruction in the empty loop and test how much time an iteration takes now. Given the clock rate of 120 MHz, how many cycles does a load instruction take?
Note that you can load from any location. An easy one is the current stack (and R1 is the stack pointer).

1.5 **Repeat with instruction cache enabled**
Now, you enabled the instruction cache and repeat Steps 1.2 through 1.4. When sending commands to the cache control registers, use proper `sync` and `isync` instructions.

1.6 **Repeat with data cache enabled**
Now, you enabled the data cache and repeat Steps 1.4. Steps 1.2 and 1.3 are not affected by data cache.

2 **Testing the configuration of data cache**
Based on your experiences from Task 1, you will design schemes to test the parameters of data cache on MPC875: the total data cache size, line size, and set associativity. You may use C language, but it is safer to use embedded instructions in core loops. Both instruction and data caches should be enabled. They are enabled after Step 1.6 anyway.

Even if you already know the structure of the data cache on MPC875, you need to reach the same conclusions from the data you collect, and explain clearly how you draw the conclusions. You can make reasonable assumptions about the parameters. For example, you can assume that the total cache size is between 1K bytes and 1M bytes. However, you cannot assume that the cache size is exactly 4K bytes.

You can discuss with other students about the testing methods, but do not copy code.

You can test the cache configuration on your desktop (or laptop) with similar methods, but this is not required.

3 **Deliverables**
Write a report adhering to the lab report requirements.